

Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A wiring of a semiconductor device comprising:
 - a first conductive layer formed on a semiconductor substrate;
 - a first insulation layer formed on said first conductive layer, wherein the first insulation layer has a scratch on a surface thereof after the surface is planarized by a CMP process;
 - a second insulation layer formed on said first insulation layer to cover the scratch formed on the surface of the first insulation layer;
 - a second conductive layer contacting said first conductive layer through a via hole formed in said first and second insulation layers; ~~said second conductive layer being a single conductive layer;~~ and
 - a groove formed in said second insulation layer over the via hole in contact with the via hole, and having a width wider than a width of the via hole, the groove having a depth less than the thickness of said second insulation layer; and
 - a third conductive layer formed in ~~in~~ the groove formed in said second insulation layer, ~~wherein said groove has a depth~~ the third conductive layer having a thickness less than ~~the~~ thickness of said second insulation layer.
2. (Original) A wiring of a semiconductor device as claimed in claim 1, wherein said first and second insulation layers are formed from a same insulation material.
3. (Original) A wiring of a semiconductor device as claimed in claim 1, wherein said

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second conductive layer comprises a plug filling said via hole.

4. (Original) A wiring of a semiconductor device as claimed in claim 1, wherein said first conductive layer is an impurity doped region on said semiconductor substrate.

5. (Original) A wiring of a semiconductor device as claimed in claim 1, further comprising:

a third insulation layer formed on said second insulation layer, having a second via hole therein; and

a fourth conductive layer formed on said third insulation layer, contacting said third conductive layer through said second via hole.

6. (Original) A wiring of a semiconductor device as claimed in claim 5, wherein said fourth conductive layer is a bit line formed from a conductive material selected from a group consisting of tungsten, aluminum and copper.

7. (Canceled)

8. (Previously Presented) A wiring of a semiconductor device as claimed in claim 1, wherein said first and second insulation layers are formed from a same insulation material.

9. (Previously Presented) A wiring of a semiconductor device as claimed in claim 1, wherein said second conductive layer is formed from a metal selected from a group consisting of tungsten, aluminum and copper.

10.-17. (Canceled)

18. (Currently Amended) A wiring of a semiconductor device comprising:
a first conductive layer formed on a semiconductor substrate;
a first insulation layer formed on said first conductive layer, a top surface of the first insulation layer being planarized by a CMP process;
a second insulation layer formed immediately over said first insulation layer and contacting said first insulation layer;
a second conductive layer contacting said first conductive layer through a via hole formed in said first and second insulation layers, ~~said second conductive layer being a single conductive layer; and~~
a groove formed in said second insulation layer over the via hole in contact with the via hole, and having a width wider than a width of the via hole, the groove having a depth less than the thickness of said second insulation layer; and
a third conductive layer formed in ~~[[a]]~~ the groove formed in said second insulation layer, ~~wherein said groove has a depth~~ the third conductive layer having a thickness less than ~~[[a]]~~ the thickness of said second insulation layer.

19. (Previously Presented) A wiring of a semiconductor device as claimed in claim 18, wherein said first and second insulation layers are formed from a same insulation material.

20. (Previously Presented) A wiring of a semiconductor device as claimed in claim 18, wherein said second conductive layer comprises a plug filling said via hole.

21. (Previously Presented) A wiring of a semiconductor device as claimed in claim 18, wherein said first conductive layer is an impurity doped region on said semiconductor substrate.

22. (Previously Presented) A wiring of a semiconductor device as claimed in claim

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18, further comprising:

a third insulation layer formed on said second insulation layer, having a second via hole therein; and

a fourth conductive layer formed on said third insulation layer, contacting said third conductive layer through said second via hole.

23. (Previously Presented) A wiring of a semiconductor device as claimed in claim 22, wherein said fourth conductive layer is a bit line formed from a conductive material selected from a group consisting of tungsten, aluminum and copper.

24. (Previously Presented) A wiring of a semiconductor device as claimed in claim 18, wherein said first and second insulation layers are formed from a same insulation material.

25. (Previously Presented) A wiring of a semiconductor device as claimed in claim 18, wherein said second conductive layer is formed from a metal selected from a group consisting of tungsten, aluminum and copper.